Process and Device Technologies for High-Performance 0.13 µm FCRAM

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We have developed a novel integration scheme for FCRAM cores using a high-dielectric capacitor technology and low-temperature process technology so we can scale the design rule towards 0.13 µm and improve device performance. Ru/Ta_2O_5/Ru capacitor technology, which can provide a dielectric constant as high as 70 and an SiO_2-equivalent thickness of 0.7 nm, has been established combined with a robust cylinder electrode fabrication process using a TiN liner. A self-aligned storage-node contact fabrication process with low-temperature (600°C) Si_3N_4 deposition improves the transistor performance by more than 10%. These technologies have been applied to a 0.13 µm-generation device, and the functionality of this device has been confirmed. Also, this paper demonstrates the scalability of these technologies to the 0.1 µm generation.

1. Introduction

Demand for System-on-a-Chip (SOC) has increased recently for use in many products such as digital AV equipment and mobile phones.[1)-4)] SOC requires the implementation of both high-performance logic and high-density embedded memory, and these requirements will be accelerated for future systems as shown in **Figure 1**. In order to satisfy these requirements, scaling of the design rule and improvement of device performance (high-speed operation) combined with the integration of high-density memory in CMOS (Complementary Metal-Oxide-Semiconductor) technology should be simultaneously achieved. Fast Cycle RAM (FCRAM)[5)] is one of the promising devices used for such systems, because high-density memory is implemented by using DRAM (Dynamic Random Access Memory) technology and its architecture is expected to provide high-speed operation.

This paper describes two key technologies developed for the DRAM core of FCRAM that make it possible to scale down design rule to 0.13 µm and improve device performance. The first of these is a new capacitor technology that meets the strong need to combine a high dielectric constant

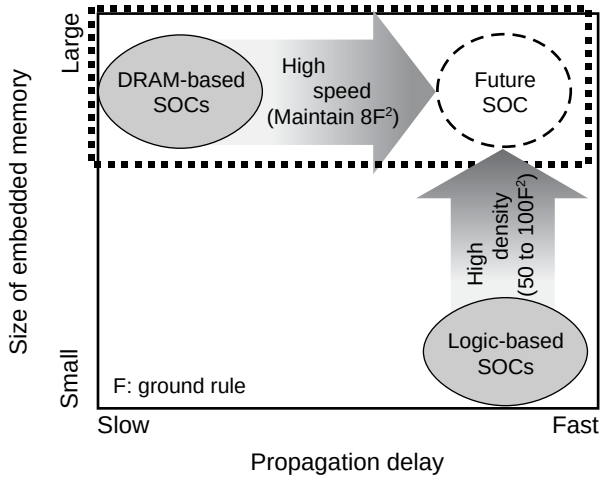


Figure 1
Development scenario toward future System-on-a-Chip (SOC). Future SOC requires the implementation of both high-performance (high-speed) and high-density embedded memory. Approach from DRAM-based SOC, which is easy to integrate with large-size memory requires improvement of operation speed.

material with a three-dimensional electrode structure.[6)-9)] The new technology[10)] uses a Metal/Insulator/Metal (MIM) capacitor with highly stable cylindrical electrodes and allows the cell size to be further reduced while maintaining the cell capacitance at around 30 fF/cell. The second key technology reduces the process temperature to prevent a degradation of MOSFET (Metal Oxide Semiconductor Field Effect Transistor) performance. A low-temperature Si_3N_4 deposition process has been integrated into a self-aligned storage-node contact process,[11)] and a greater than 10% improvement of transistor performance has been achieved.[12)] These technologies have been fully integrated in a 0.13 µm test device and their potential usefulness has been confirmed. This paper also describes the scalability of these technologies toward the 0.1 µm generation.

2. Ru/Ta_2O_5/Ru capacitor with liner-supported cylinder (LSC) technology

In the conventional capacitor technology for a DRAM core, the combination of a silicon oxynitride dielectric film and a doped poly-silicon electrode material has been widely utilized. Since the design rule has been scaled down, there has been a wide demand for a capacitor technology that uses a high dielectric constant material and a three-dimensional electrode capacitor.[6)-9)] One of the most promising capacitor structures with a high dielectric constant is the metal/Ta_2O_5/metal capacitor (MIM-Ta_2O_5 capacitor) with Ru metal electrodes.[13),14)]

When Ru is used for the top and bottom metal electrodes of an MIM-Ta_2O_5 capacitor, this system displays better performance than when TiN and WN electrodes are used, with a dielectric constant of around 70 and an SiO_2-equivalent thickness of 0.7 nm (**Figure 2**).[15)-18)] However, until now, stable formation of cylindrical bottom electrodes with Ru has been impossible because of two reasons. Firstly, the adhesion of Ru and SiO_2 is so poor that wet-etchant penetrates along the interface during the sacrificial-SiO_2 strip process and severely attacks the stopper-Si_3N_4 {**Figure 3 (a)**}, causing the collapse of the cylinder electrodes. Secondly, oxygen can penetrate the Ru film so easily that the surface of the contact plug material would be oxidized in the oxidizing ambient of Ta_2O_5 formation, causing contact failures {**Figure 3 (b)**}.

These problems were overcome by using the Liner-Supported Cylinder (LSC) technology with a TiN-liner formed in the shape of a calyx.[10)] **Figure 4** shows the process flow of LSC tech-

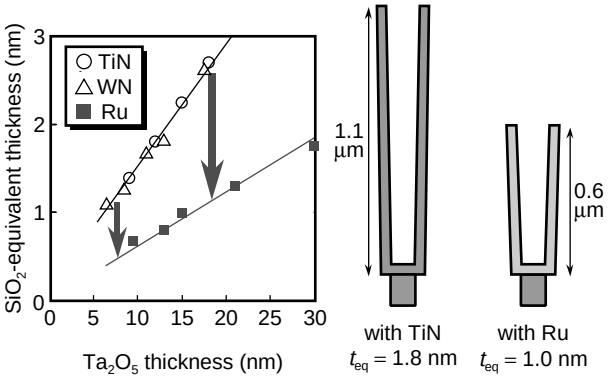


Figure 2
Impact of electrode material selection in metal/Ta_2O_5/metal capacitor. By using Ru electrodes, SiO_2 equivalent thickness can be reduced and lower electrodes can be expected.

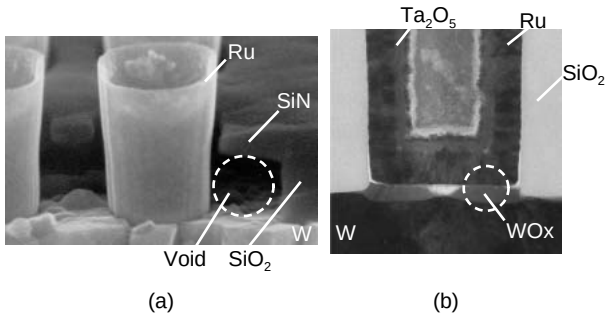


Figure 3
Difficulties with Ru cylinder electrodes. (a) Adhesion of Ru and SiO_2 is so poor that wet-etchant penetrates along the interface during sacrificial-SiO_2 strip process and voids and cylinder collapses occur. (b) Oxygen easily penetrates through Ru electrode; therefore, plug W is oxidized, causing a contact problem.

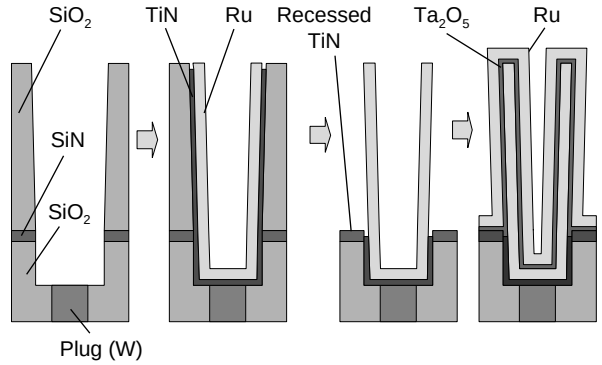
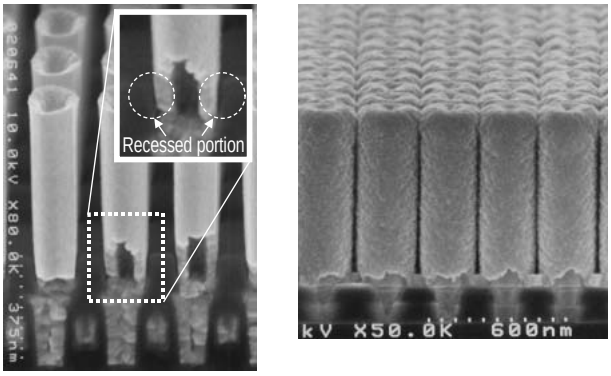


Figure 4
Process flow of LSC capacitor.



(a) (b)

Figure 5
Cross-sectional view of LSC capacitor fabricated with 0.13 µm rule. (a) Photograph after liner TiN strip and recess process. (b) Photograph after plate electrode formation.

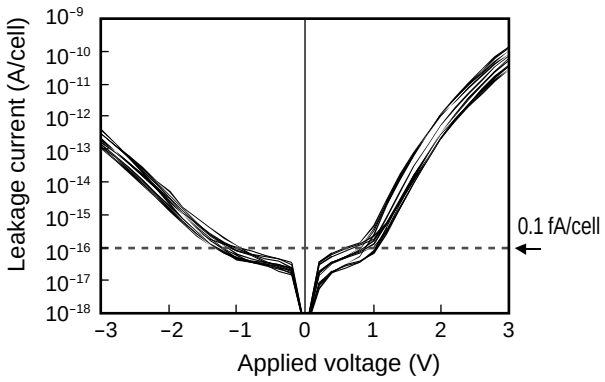


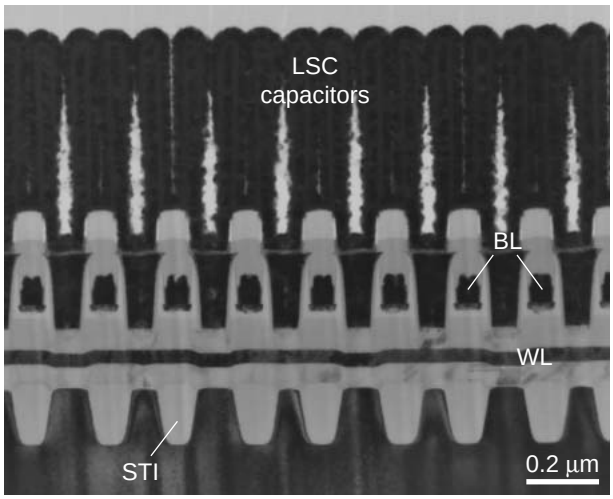
Figure 6
Leakage current and applied voltage characteristics of LSC capacitor.

nology. TiN, Ru, and Ta_2O_5 are deposited by CVD (Chemical Vapor Deposition) using $TiCl_4$, $Ru(EtCp)_2$, and $Ta(OC_2H_5)_5$ as the source materials, respectively. All processes are performed at a temperature below 600°C. The key processes of this technology are the formation of the thin TiN liner and its removal by well-controlled wet etching with diluted H_2SO_4/H_2O_2. After this wet etching, the liner TiN is slightly recessed below the surface of the support-SiO_2 to the designed depth so that the electrical characteristics of the capacitor are not affected. The TiN-liner acts both as an adhesion layer between the Ru and SiO_2 and as an oxidization barrier during Ta_2O_5 formation. **Figure 5** shows a cross-sectional view of a sample fabricated with a 0.13 µm ground rule and 550 nm-high cylinder capacitors that were successfully built without any collapses.

Figure 6 shows the I-V characteristics of the LSC-Ta_2O_5 capacitor. The leakage current of this capacitor is below 0.1 fA/cell over the range of −0.8 to 0.8 V, which is low enough for DRAM applications. The LSC technology was applied to a fully integrated 0.13 µm test device combined with other key technologies such as optimized KrF (Krypton Fluoride) excimer laser lithography,[19] a poly-metal gate transistor,[20),21] and a dual-damascene bit-line process.[11] A TEM image of the fully integrated device is shown in **Figure 7**. The DRAM functionality was confirmed on 256 kbit test devices.

Next, we will discuss the scalability of LSC capacitor technology. To maintain a capacitance of 30 fF/cell, we plotted the required aspect ratios of the storage-node electrode as a function of the device design rule with various SiO_2-equivalent thicknesses of Ta_2O_5 (**Figure 8**). The realistic aspect ratio was assumed to be less than 8,

considering the via-hole opening and filling by the sides of the capacitors. Compared with other bottom electrode materials such as TiN, Ru with the LSC technology is much better able to bring out the best Ta_2O_5 performance, resulting in a scalability towards sub-0.10 µm generations. A cross-sectional view of a device scaled down to a 0.11 µm design rule is shown in **Figure 9**, indicating that scaling is feasible.



BL: Bit line
WL: Word line
STI: Shallow trench isolation

Figure 7
Cross-sectional TEM image of a fully integrated 0.13 µm test DRAM.

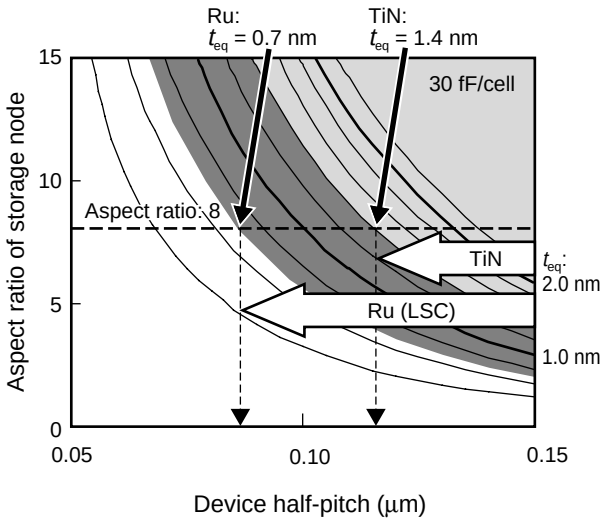


Figure 8
Scalability of LSC capacitor. Aspect ratio of the storage node is plotted as a function of device half-pitch (design rule). Required capacitance and realistic aspect ratio of storage node are assumed to be 30 fF/cell and 8, respectively. LSC technology with Ru electrodes will be scaled to below 0.1 µm generation.

3. Impact of thermal budget reduction on MOSFET performance and integration with low-temperature process

The high-temperature process after MOSFET fabrication leads to impurity deactivation in the source and drain regions, which eventually degrades MOSFET performance by reducing the drain current. Conventionally, the temperature has been highest in the capacitor fabrication process and the CVD Si_3N_4 deposition process used in a self-aligned contact (SAC) formation. These high-temperature processes should be avoided in the processes for high-performance SOCs. The LSC capacitor technology presented in the previous chapter has lowered the process temperature to below 600°C, which is more than 100 to 200°C below that of the conventional capacitor process. The remaining high-temperature process is Si_3N_4 deposition.

Figure 10 shows a schematic drawing of a DRAM structure after capacitor formation. A tungsten poly-metal gate and tri-layer barrier metal technology for a tungsten contact[11] were employed. To create a self-aligned storage node contact, CVD-Si_3N_4 films with good step-coverage

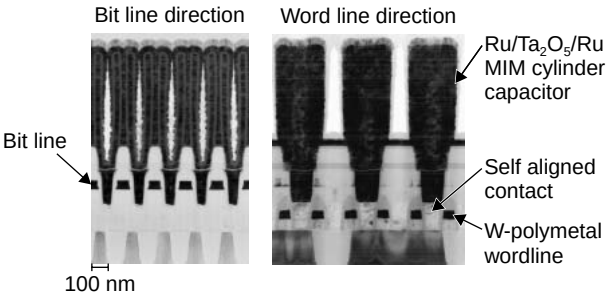


Figure 9
Cross-sectional images of device scaled down to 0.11 µm design rule.

were used as an etching stopper for the bit-line cap and sidewalls. Although use of CVD-Si_3N_4 is attractive because of its high step-coverage, its high-temperature and long-lasting thermal sequence drastically increases the thermal budget after final activation and degrades device performance. We overcame this problem by applying a low-temperature CVD-Si_3N_4 technology together with a hexachlorodisilane (HCD) gas source[22] instead of the conventional dichlorosilane (DCS) source. This approach lowered the process temperature from more than 700°C to less than 650°C. **Table 1** compares the thermal budgets for different CVD-Si_3N_4 deposition processes. By using HCD-Si_3N_4, we can lower the process temperature to between 600 and 650°C without extending the treatment time.

Figure 11 shows the leakage current distribution between the bit line (BL) and the storage node (SN) as measured using a 4M-bit test vehicle over all parts of a wafer to which the low-temperature HCD-Si_3N_4 was applied as an SAC etching stopper. No SN-BL shorts caused by the

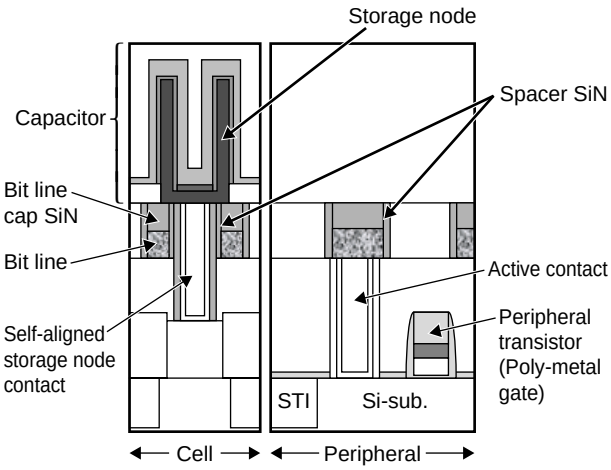


Figure 10
Schematic of DRAM structure after capacitor formation.

Table 1
Comparison of thermal budgets for different CVD-Si_3N_4 deposition processes.

	DCS-Si_3N_4	HCD-Si_3N_4	
Growth temp. (°C)	700	650	600
Process time (min)	541	206	304

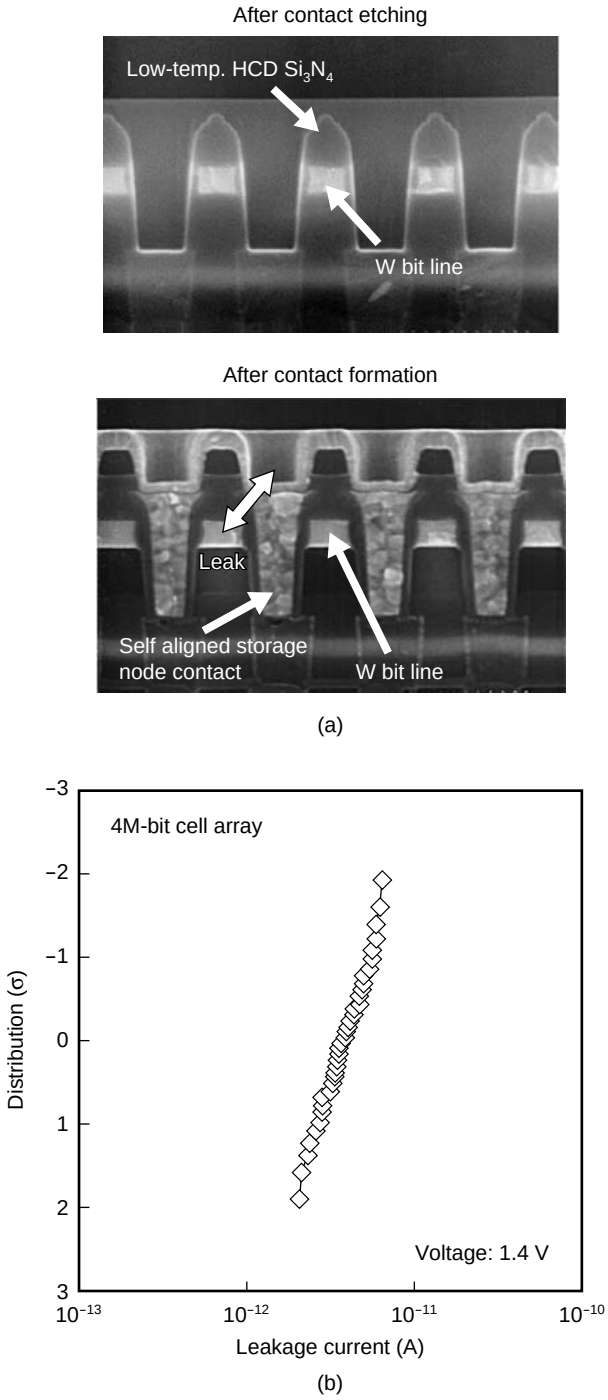


Figure 11
(a) Photograph of self-aligned storage node contact formation using low-temperature HCD-Si_3N_4. (b) Distribution of leakage current between bit line and storage node as measured by 4M-bit cell array monitor.

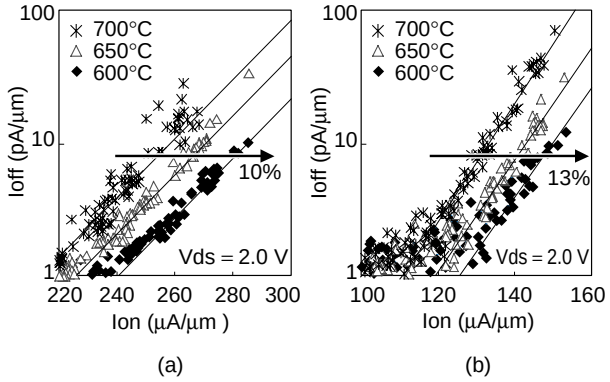


Figure 12
Relation between Ion and Ioff for different thermal process temperatures. More than 10% increase of Ion was observed for both the NMOSFET (a) and PMOSFET (b) at a fixed Ioff.

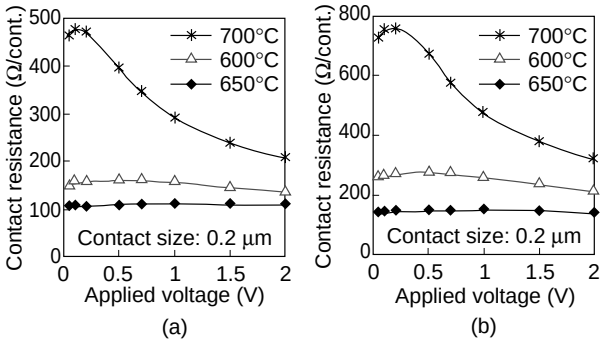


Figure 13
Active N^+ (a) and P^+ (b) contact resistance as a function of applied voltage for different process temperatures. By reducing the process temperature, not only the contact resistance but also the non-linearity is improved.

SAC process were observed, also indicating the adequate selectivity of the HCD-Si_3N_4 film during SAC etching.

The impact of lowering the process temperature was clarified by measuring peripheral MOSFET devices with a 5.2 nm-thick gate dielectric. **Figure 12** shows the Ion vs. Ioff characteristics for NMOSFET and PMOSFET devices at Vds = 2.0 V under different thermal process temperatures. In this figure, a process temperature of 600°C indicates that the maximum process temperature is limited by the MIM-Ta_2O_5 capacitor fabrication process. Also, temperatures above 600°C indicate that the temperature is highest in the CVD-Si_3N_4 deposition process. It is clear that lowering the process temperature has a strong impact on performance. By using 600°C as the process temperature, the drive currents of the NMOSFET and PMOSFET devices at Ioff = 10 pA/µm were improved, respectively, by about 10% and 13%, compared to those of the conventional Si_3N_4 process at 700°C. This improvement seems mostly due to the reduction of dopant deactivation.

Figure 13 shows the active contact resistance as a function of applied voltage. In the 700°C process, the contact resistance to the N^+ and P^+ diffusions increased drastically as the applied voltage was decreased; that is, these contacts show strong non-linear characteristics even though a thermally stable metal-contact process was used.[4] This non-linearity sometimes became a serious problem in circuit design. The non-linear characteristics originate from a low active-dopant concentration at the surface of the N^+ and P^+ diffusions. By lowering the process temperature from 700°C to below 600°C, we significantly improved not only the contact resistance but also the ohmic characteristics of the contacts, resulting in less deterioration of transistor performance. The sheet resistances of N^+ and P^+ diffusions also indicate less dopant deactivation when a low-temperature process is used.

In order to evaluate circuit performance for a low-temperature nitride process, we measured the propagation delay time (T_{pd}) of an inverter ring oscillator. A time of 125 ps was obtained for T_{pd} at a fan-out of 3, and this value meets the device target. We also checked the scalability of this low-temperature process to next-generation devices, which we assume will have a 0.11 µm design rule, by simulating the propagation delay time (**Figure 14**). In the next generation, we assume that the gate length (Lg) and gate oxide thickness (Tox) will be scaled down and the supply voltage (Vcc) will be reduced. Even if we reduce the supply voltage to 1.2 V, a propagation delay time of

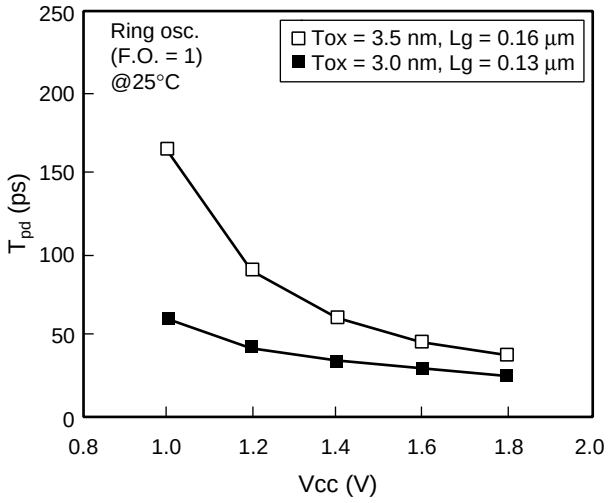


Figure 14
Simulated propagation delay time (T_{pd}) for scaled design rule. Gate length was scaled to 0.13 µm, and gate oxide thickness was scaled to 3.0 nm.

45 ps can be obtained at a fan-out of 1. This suggests that the technology presented here will also be usable in the next generation and is promising for device scaling.

4. Conclusion

This paper described some key technologies for a 0.13 µm-rule FCRAM core with high-performance MOSFET characteristics. A newly developed LSC capacitor technology enables us to fabricate robust Ru/Ta_2O_5/Ru cylinder capacitors at low temperature. The impact of lower process temperatures on device performance was also clarified. By applying a low-temperature Si_3N_4 deposition process to a self-aligned contact process, deterioration of peripheral MOSFET device performance was effectively suppressed. Furthermore, the scalability of these technologies to the 0.1 µm era was also demonstrated. This technology is a promising candidate for application in future SOC fabrication.

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